SEMICONDUCTOR DEVICES II:
Advanced nm-channel CMOS devices (FinFET, UTB SOI, 2D materials, 3D integration) – Part I
Lecture #3

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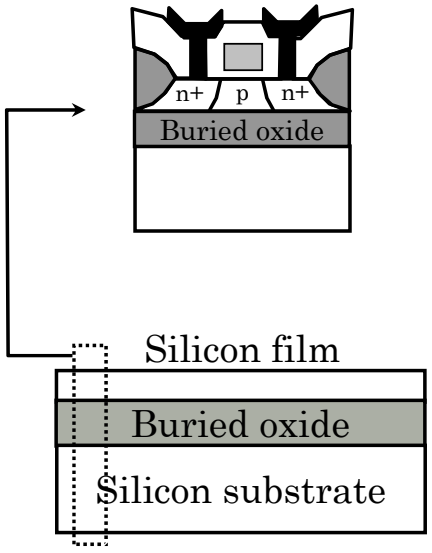
Outline

- **MOSFET principle and scaling:**
  - Operation and main figures of merit
  - Dennard happy scaling @ constant electric field
  - Short channel effects and DIBL MOSFETs
  - Saturation and output conductance
- **Nanometer CMOS:**
  - **Technology boosters below 100nm**
  - **FinFETs**
  - **Silicon On Insulator**
  - **Ultra Thin Body SOI MOSFET**
  - **Nanowire MOSFET**
  - **2D MOSFETs**
  - **3D integration**

Silicon-On-Insulator (SOI) Substrates

SOI MOSFET



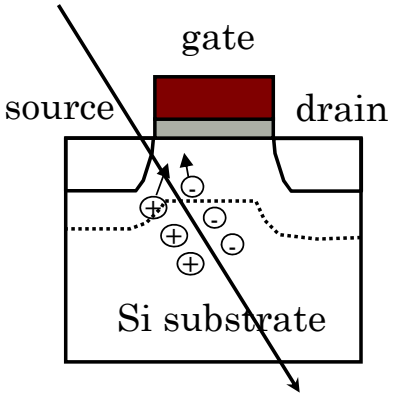
SOI wafer

Why ?

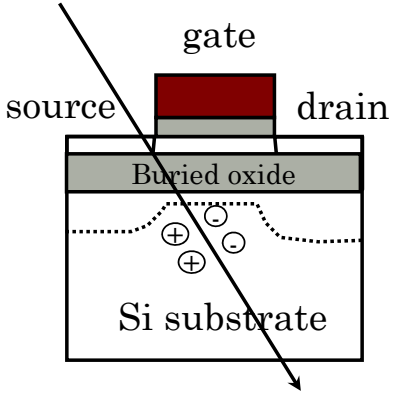
- Historically: → rad-hard devices
- Better lateral isolation, compact solution
- Less parasitic capacitances
- Reduced junction leakage
- Better short channel effects
- 3D integration possible

Today SOI → low-voltage, high-speed, RF

Bulk Si: Ionizing radiation affects charges in the channel



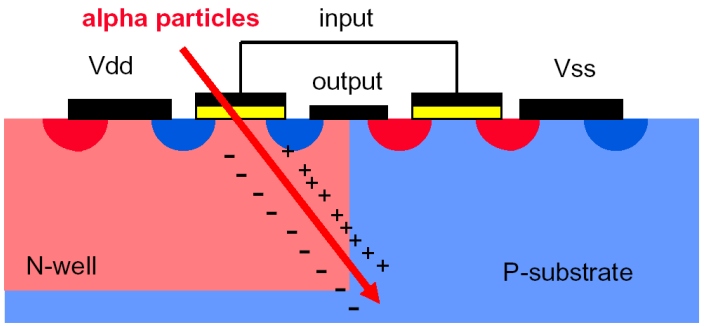
SOI: Ionizing radiation generated charges are isolated below the buried oxide



Naturally less sensitive to ionizing radiation

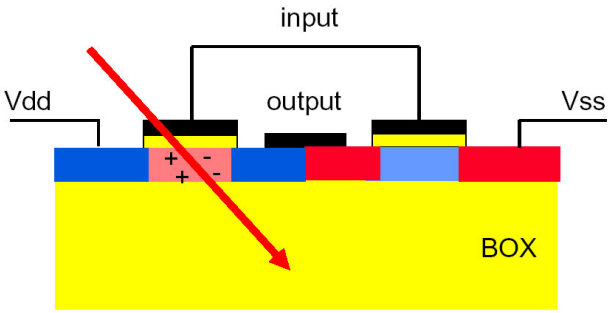
Less soft errors in SOI inverter than in bulk CMOS

soft errors in bulk CMOS



Alpha particles ➡ "soft" errors

soft errors in SOI



Low soft error rate

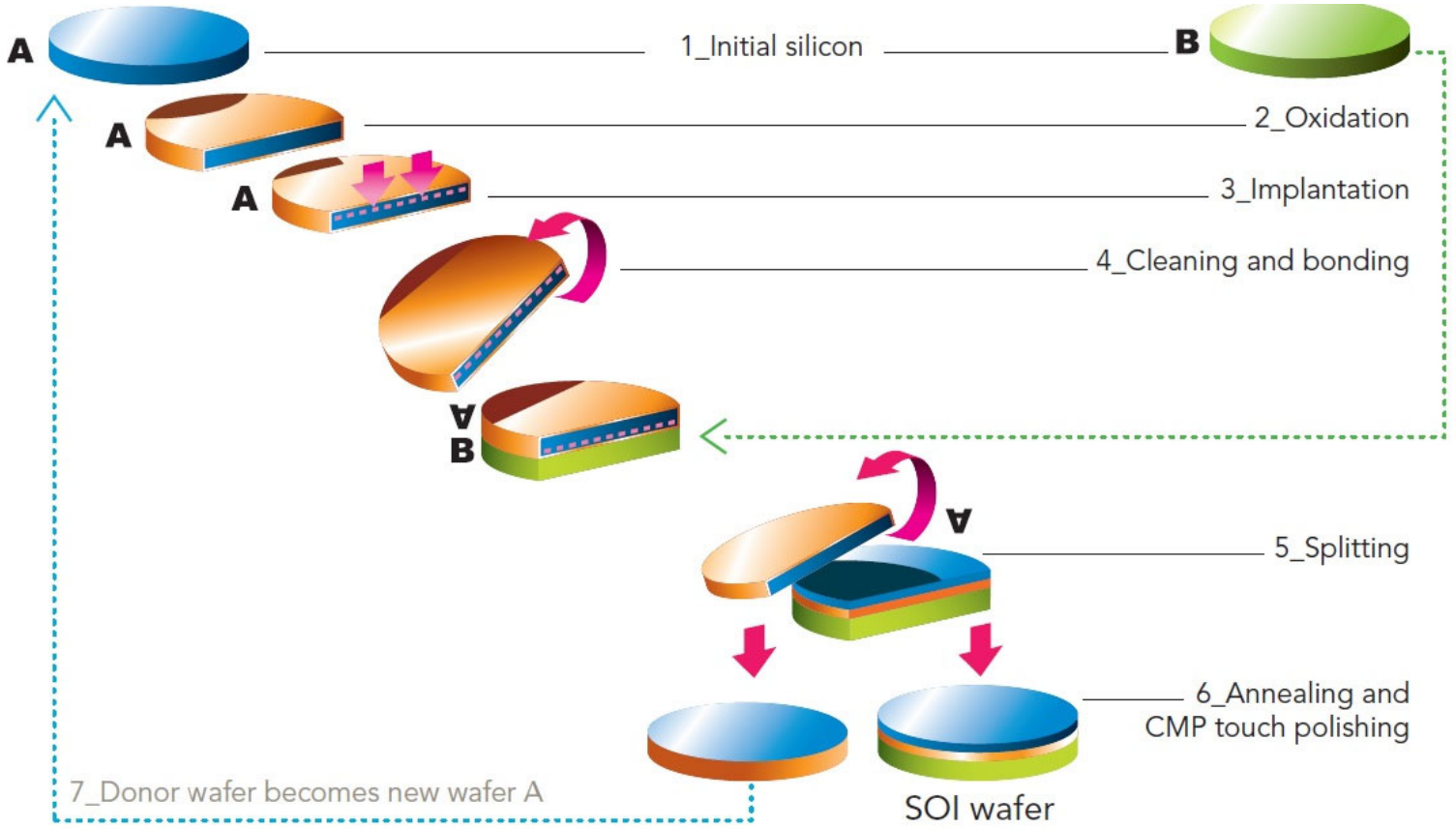
Sources of alpha particles ➡ Generate soft errors

- Cosmic Rays (aircraft electronics vulnerable)
- Decaying uranium and thorium impurities in integrated circuit interconnect

Generates electron-hole pairs in substrate

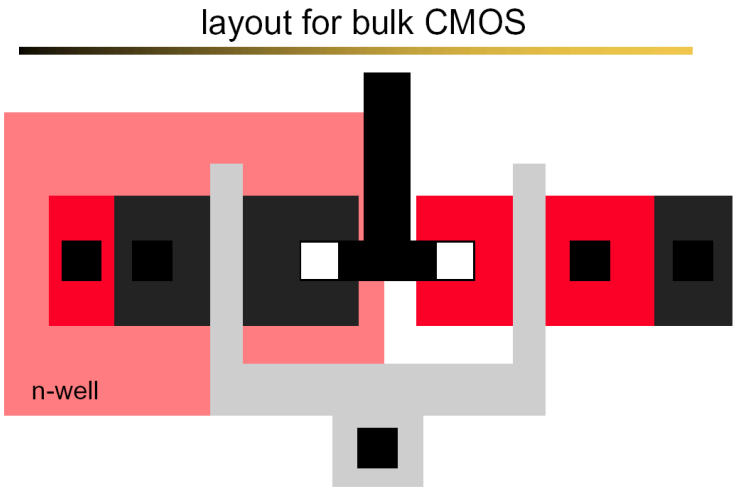
- Excess carriers collected by diffusion terminals of transistors
- Can cause upset of state nodes – floating nodes, DRAM cells most vulnerable

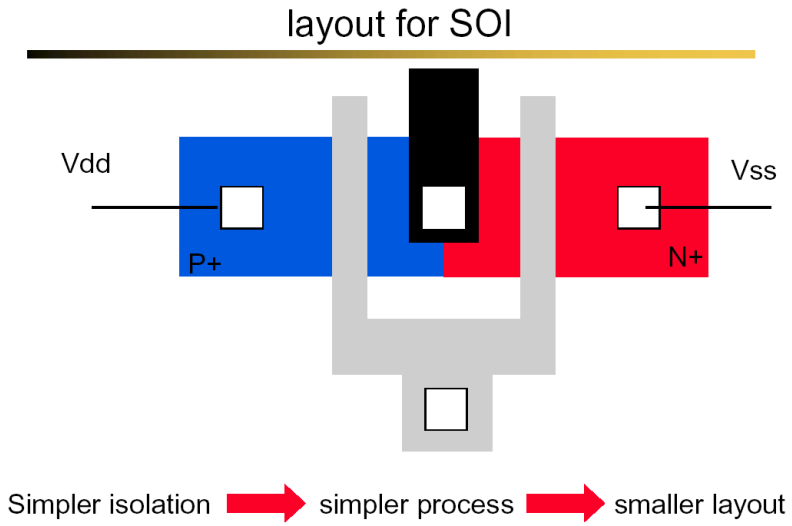
Smartcut process for Silicon On Insulator substrates © SOITEC

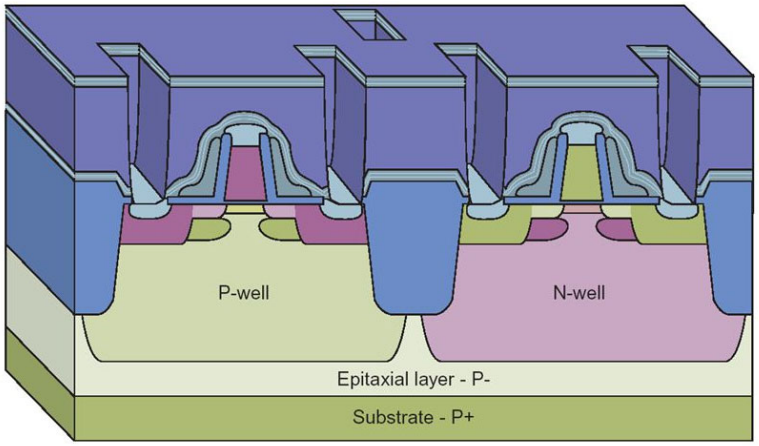


Invented by CEA-LETI & SOITEC, Bernin, France

SOI versus bulk CMOS inverter design







LESS MASKS, LESS COMPLEX PROCESS,
MUCH COMPACT, SMALLER AREA

SOI Wafers: state of the art in thin film SOI

Fully-depleted Silicon-on-Insulator (FD-SOI) – substrates

- The prevalent method for FD-SOI substrate manufacture uses the "SmartCut" process, licensed by SOITEC to wafer suppliers.

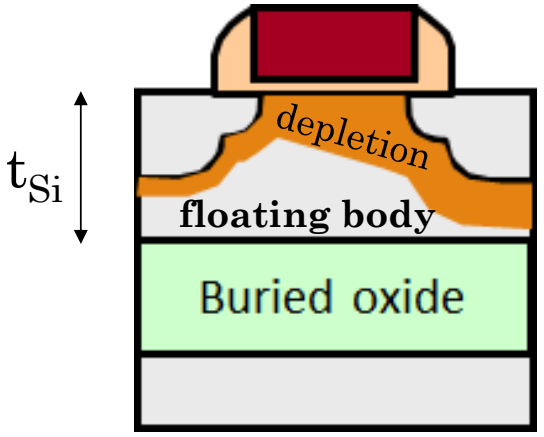
For the 28nm node, the uniformity of the thin Silicon layer is +/- 5A over the 300mm wafer, equivalent to 0.2" between Chicago and San Francisco.

http://www.soitec.com/en/products-and-services/microelectronics/fd-2d/

Partially Depleted (PD) SOI MOSFET

- **Si thickness is higher than the depletion depth → PD, neutral body**

+ similar to bulk-Si
+ no coupling of top and bottom Si/SiO2 interfaces
- Short channel effects (SCE): as in bulk, no real advantage
- floating body (no electrical contact)
- Kink effect (in Id-Vd characteristics)
- dynamic over- and under-shoots
- self-heating effects (SHE)

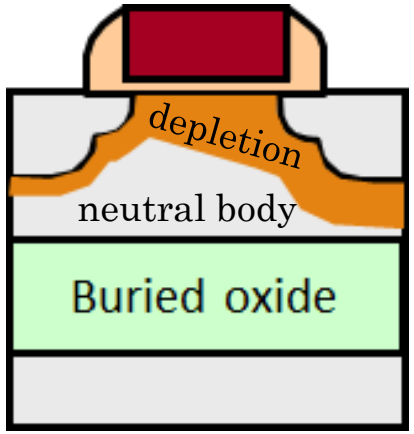


$t_{Si} > W_{dep}$

Remarks:
- CMOS easier to manufacture in PD SOI: used for power PC by IBM
- but no significant advantage for nanometer scaling
- unless the body is tied electrically to the source → **floating body effects**

Partially Depleted (PD) SOI MOSFET: What is floating body effect

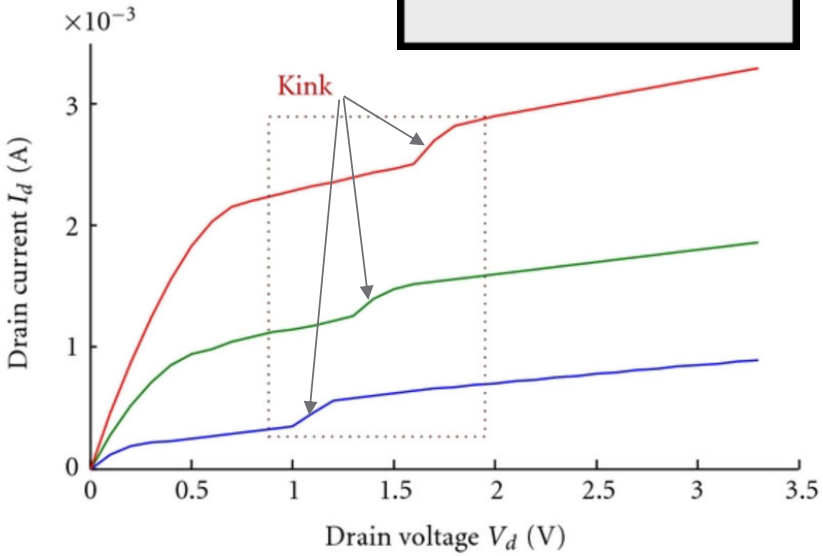
$$T_{SOI} > W_T, \text{ where } W_T = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_{body}}}$$



Floating body effect (*history dependent*):

- When a PD-SOI NMOSFET is in the ON state, at moderate-to-high V_{DS}, holes are generated via impact ionization near the drain.
- Holes are swept into the neutral body, collecting at the source junction.
- The body-source pn junction becomes forward biased:

→ V_T is lowered → I_{Dsat} increases → **"kink" in output I_D *vs.* V_{DS} curve**



Fully Depleted (FD) SOI MOSFET

$$T_{SOI} < W_T, \text{ where } W_T = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_{body}}}$$

+ Excellent control of short channel effects

+ No floating body effect

+ Less capacitance parasitics

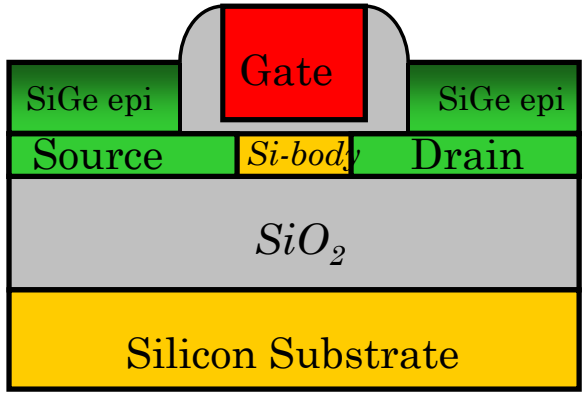
+ Less junction leakage

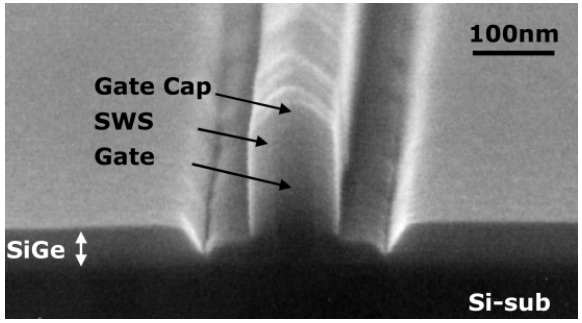
+ Quasi-ideal subthreshold swing

- V_T is sensitive to SOI film thickness

- Elevated (or recessed) S/D contact structure needed to reduce series resistances, R_S, R_D

- Self heating effects





Body Factor in FD SOI MOSFET

Body factor in bulk-Si MOSFET

$$m = 1 + \frac{\varepsilon_{si}}{C_{ox} X_{d\max}} \cong 1.4 \text{ to } 1.6, \text{ typically} \qquad (2)$$

where $X_{d\max}$ is the maximum depletion width in strong inversion.

In a SOI FD MOS transistor, on the other hand, the body effect is given by **Body factor in FD SOI**

$$m = 1 + \frac{\frac{\varepsilon_{si}}{t_{si}} C_{oxb}}{C_{ox}\left[\frac{\varepsilon_{si}}{t_{si}} + C_{oxb}\right]} \cong 1.05 \text{ to } 1.1 \text{ typically} \qquad (3)$$

where C_{ox}, C_{oxb} and t_{si} are the gate oxide capacitance, the buried oxide capacitance and the silicon film thickness, respectively. From the above equations, it follows that the saturation drain current may be 30–40% higher in a FD SOI device than in a bulk device with similar parameters [3].

Analog performace better in SOI:

Transconductance/ drain current ratio gm/ID:

$$\frac{g_m}{I_D} = \frac{dI_D}{I_D dV_G} = \frac{\ln(10)}{S} = \frac{q}{nkT} \qquad (5)$$

The low body-effect coefficient of SOI devices thus allows for obtaining near-optimal micropower designs (g_m/I_D values of $35\,V^{-1}$ are obtained, while g_m/I_D reaches only values of $25\,V^{-1}$ in bulk MOSFETs). [9,10,19]

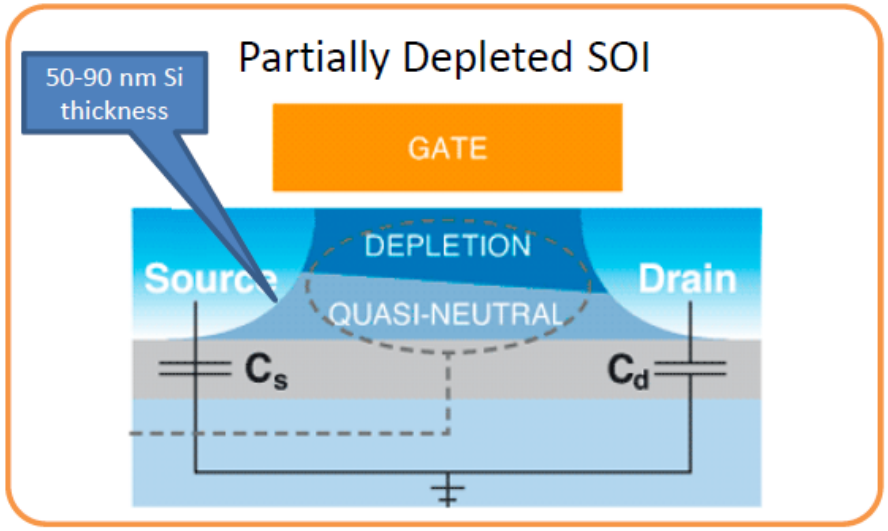
In strong inversion, the g_m/I_D becomes (for long-channel devices):

$$\frac{g_m}{I_D} = \sqrt{\frac{2 \cdot \mu \cdot C_{ox} \cdot W/L}{n \cdot I_D}} \qquad (6)$$

and will still remain higher in FD SOI than in bulk MOSFETs with similar technological characteristics.

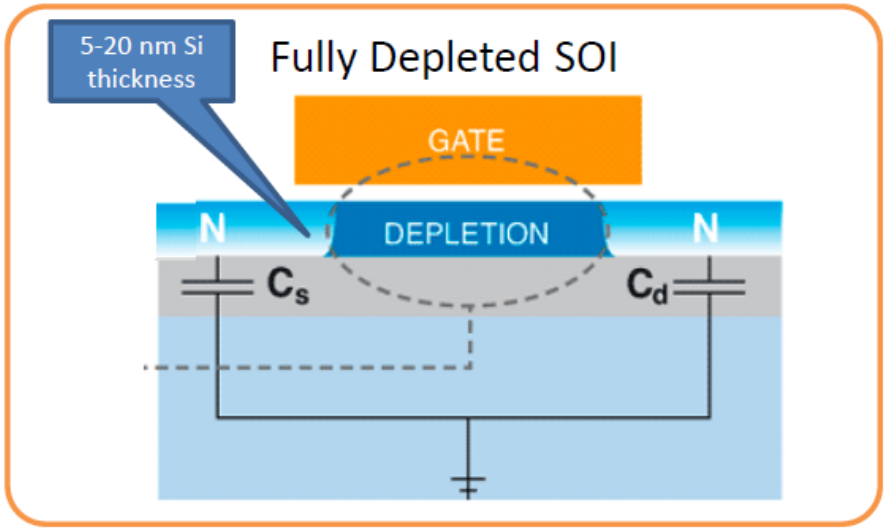
Summary: Fully Depleted (FD) versus Partially Depleted (PD) SOI MOSFET

PD-SOI



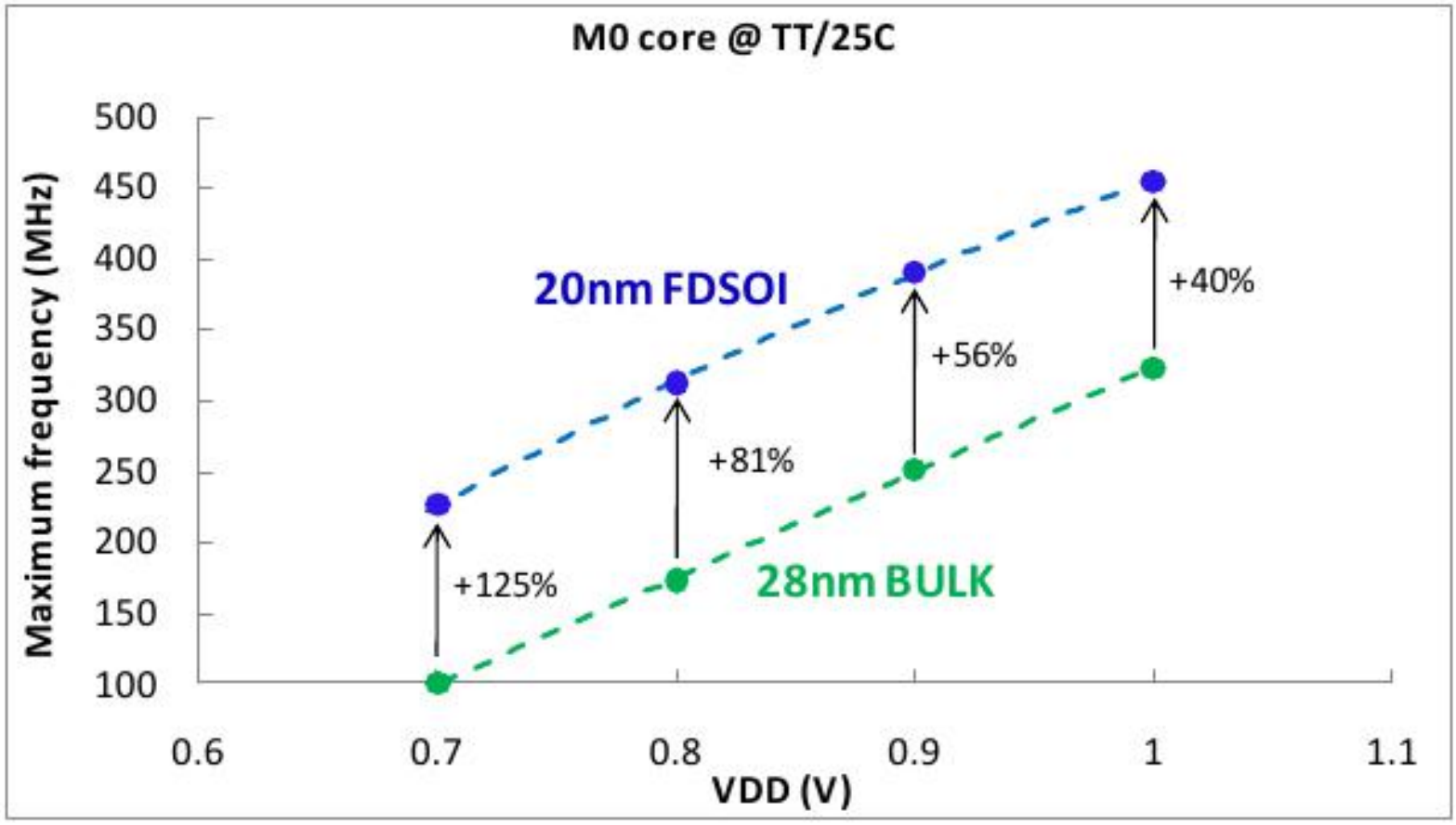
Works for rad-hard applications, similar design to bulk, no SCE advantages

FD-SOI



Best solution for nanometer scaling and low power, reduces significantly SCE, near 60mV/dec SS

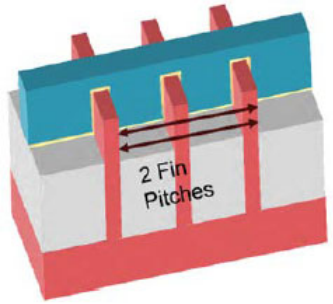
FD SOI CMOS versus Bulk CMOS performance

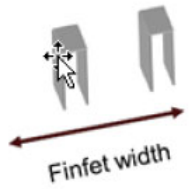


Fin FET versus FD SOI MOSFET

The only two remaining inudstrial technology options for sub-10 nm scaling are FinFETs and FD SOI MOSFETs, followed by 1D/2D transistors (these last ones are under research).

Category	FinFet	FD-SOI
Base Wafer Cost		x4
Process Complexity	↑	↓
Overall Wafer Cost	→ to ↗	→ To ↘
Die Yields	??????	??????
Unit Cost	??????	??????
Process control & metrology challenges	↑	↓
Active transistor area density	↑	↓
Performance (Ion vs. Ioff)	Similar	Similar

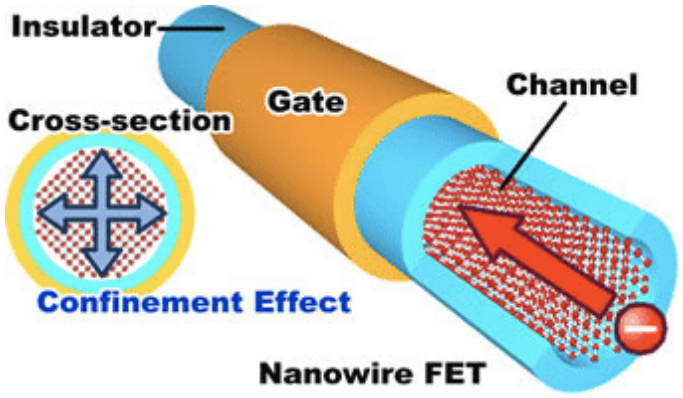


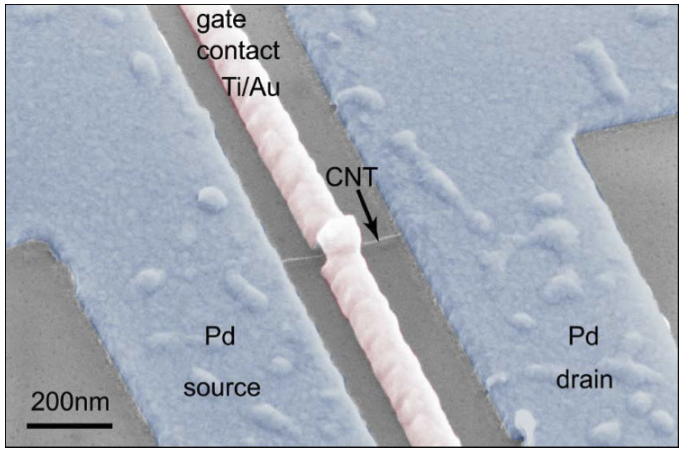


1D (nanowire) FETs

Why **semiconducting nanowires (NWs)** and **carbon nanotubes** (CNTs):

- due to their **potential to test fundamental concepts** about dimensionality
- can serve as basic **building blocks of emerging technology platforms**
- enable **new integrated functionality** in highly dense low cost integrated circuits
- use advanced existing fabrication schemes: **Si-toolset with** tunable electrical properties by **controlled doping**
- **predictable electron transport**: enhanced engineering of device characteristics
- well-defined surface structural properties: **enhanced interfacial engineering**
- **Vertical and lateral isolation** possible with SOI devices

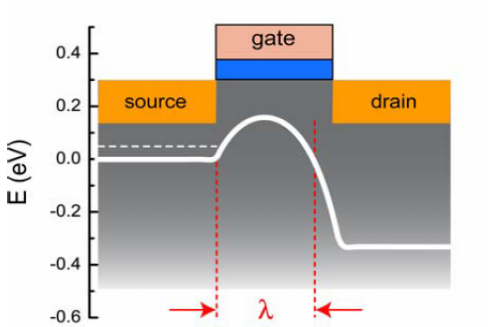




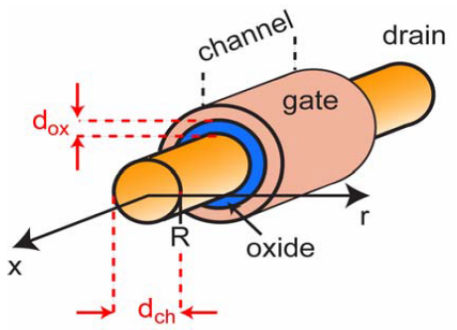
Electrostatics of nanowire FET vs. planar MOSFET

Comparison of Planar vs. Nanowire Architecture

Planar MOSFET



Nanowire MOSFET:



- **Planar gate:**
  limited electrostatic control of the channel

$$\lambda = \sqrt{\frac{\varepsilon_{ch}}{\varepsilon_{ox}} d_{ox} d_{channel}}$$

- **Example:**
  8nm SOI, 1 nm SiO2: $\lambda \approx 5$ nm
  $\Rightarrow$ $L_G > 20$ nm

- **Surround gate (Nanowire):**
  ultimate electrostatic control of channel

$$\lambda = \sqrt{\frac{\varepsilon_{nw} d_{nw}^2 \ln\left(1 + \frac{2d_{ox}}{d_{nw}}\right)}{8\varepsilon_{ox}}}$$

- **Example:**
  8 nm SiNW 1 nm SiO_2: $\lambda \approx 2.3$ nm
  $\Rightarrow$ $L_G > 9$ nm

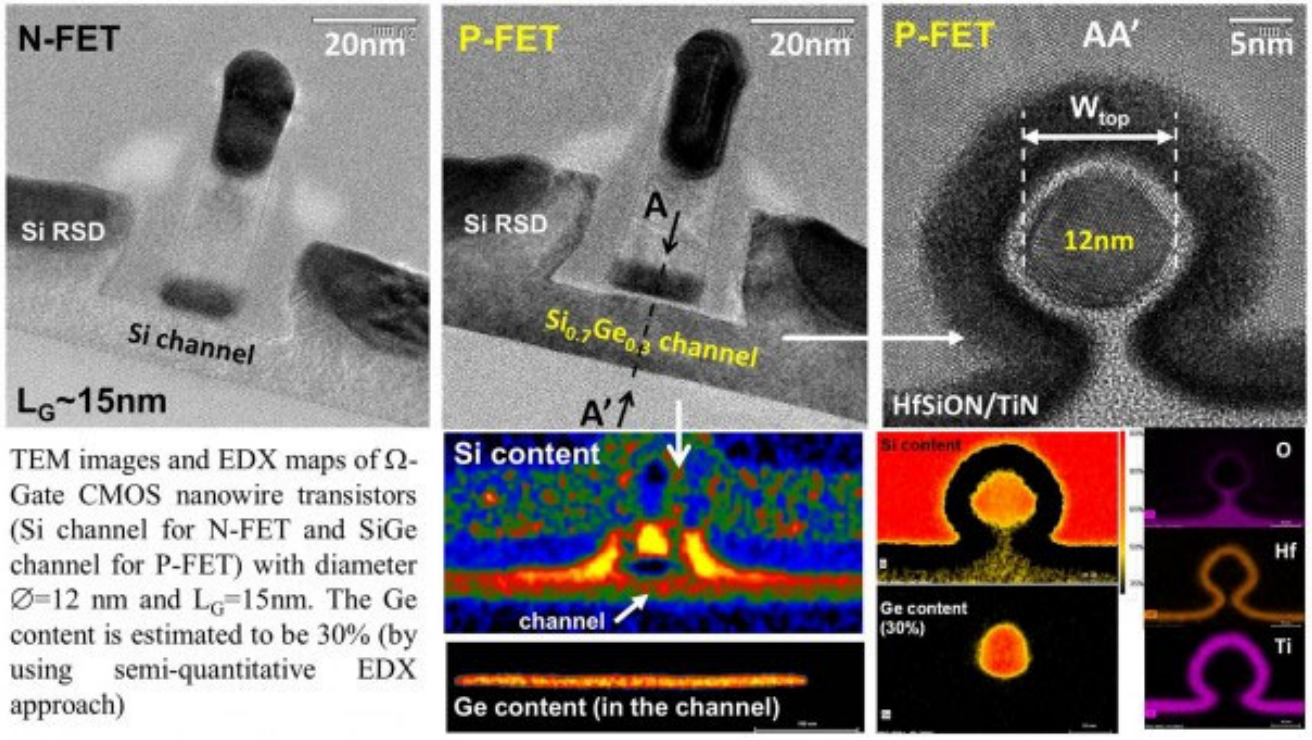
⇨ **NW device geometry yields improved scaling and better inv. subthreshold slope**

Source: Heike Riel, IBM.

15nm nanowire FET – by top down lithography

Dual-Channel CMOS Co-Integration with Si Channel NFET and Strained-SiGe Channel PFET in Nanowire Device Architecture Featuring 15nm Gate Length

P. Nguyen et al (Leti, ST, Soitec) – IEDM 2014.

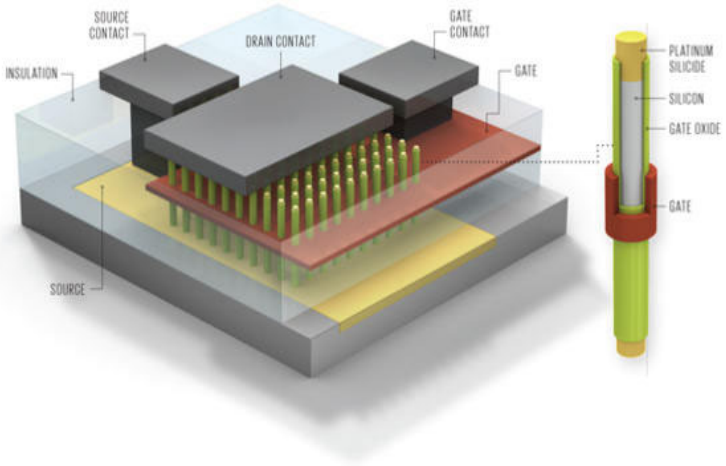


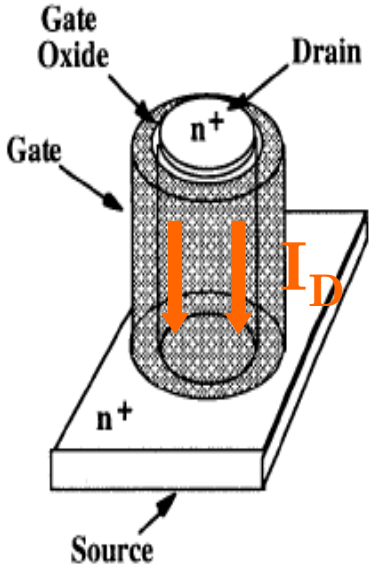
TEM images and EDX maps of Ω-Gate CMOS nanowire transistors (Si channel for N-FET and SiGe channel for P-FET) with diameter ∅=12 nm and L_G=15nm. The Ge content is estimated to be 30% (by using semi-quantitative EDX approach)

- 687μA/μm for p-FET
  647μA/μm for n-FET
  @ VDD=0.9V
- with low leakage current
- excellent short-channel-control & DIBL<50mV/V

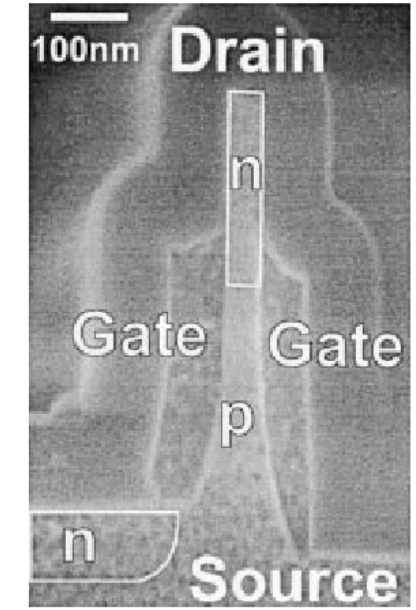
Vertical nanowire MOSFETs

- Idea: **channel length is defined by the thickness of a semiconductor material**
- Design: **VERTICAL**, contacts at top & bottom (source / drain = bottom / top or vice-versa)
- Performance: similar to 1D NW MOSFET
- Advantage: more dense (very suitable for memory)





Infineon's first vertical MOSFET



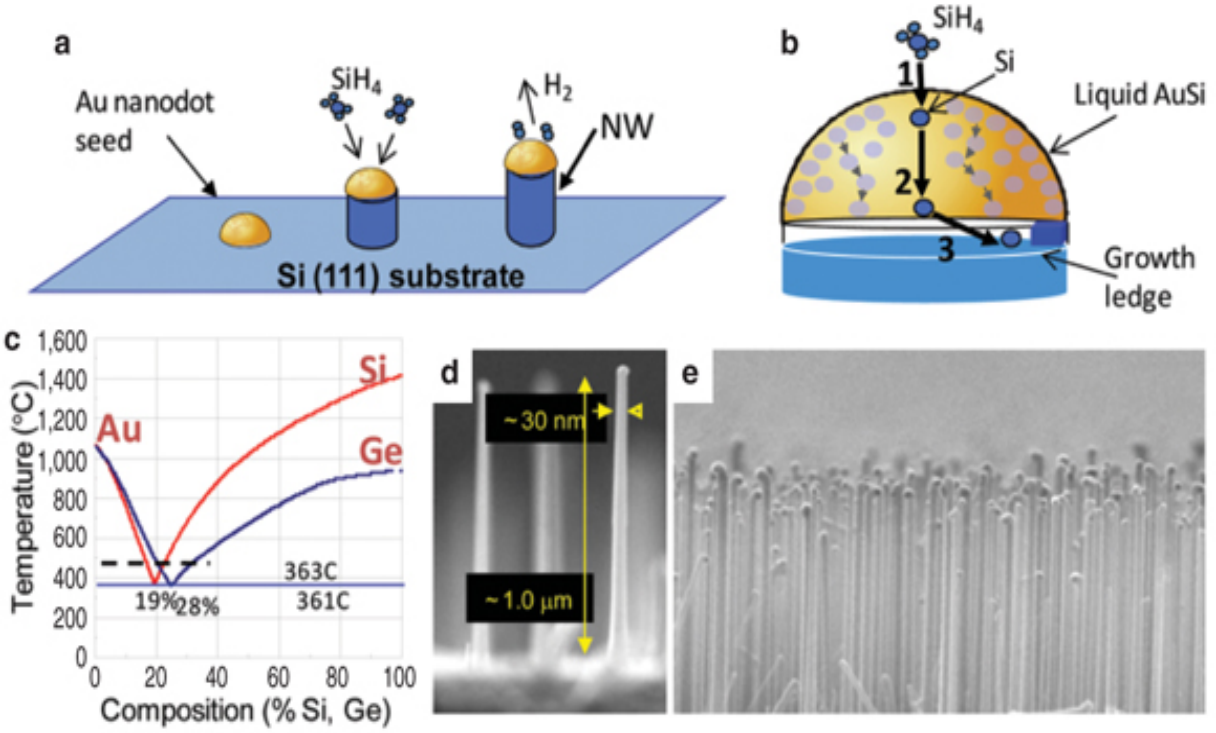
Application: SRAM

T. Schulz et al., IEEE TED, August 2001.

Bottom-up nanowires by Vapor-Liquid-Solid (VLS) Growth

VLS Growth Technique

- **Gas precursor molecules** or vapor containing the growth species are introduced into a furnace or chemical vapor deposition (CVD) reactor and liquid metal catalysts on a surface react with the source atoms to grow nanowires.
- **A metal nanodot** catalyzes the growth of the nanowire from a vapor source by forming a liquid metal droplet through which the growth atoms are transported to the crystallizing interface. The catalytic seed floats on top of the nanowire and defines the nanowire diameter while the growth rate kinetics together with the growth time defines the nanowire length.
- **The nanowire 'self-assembles' in a bottom-up synthesis technique.**



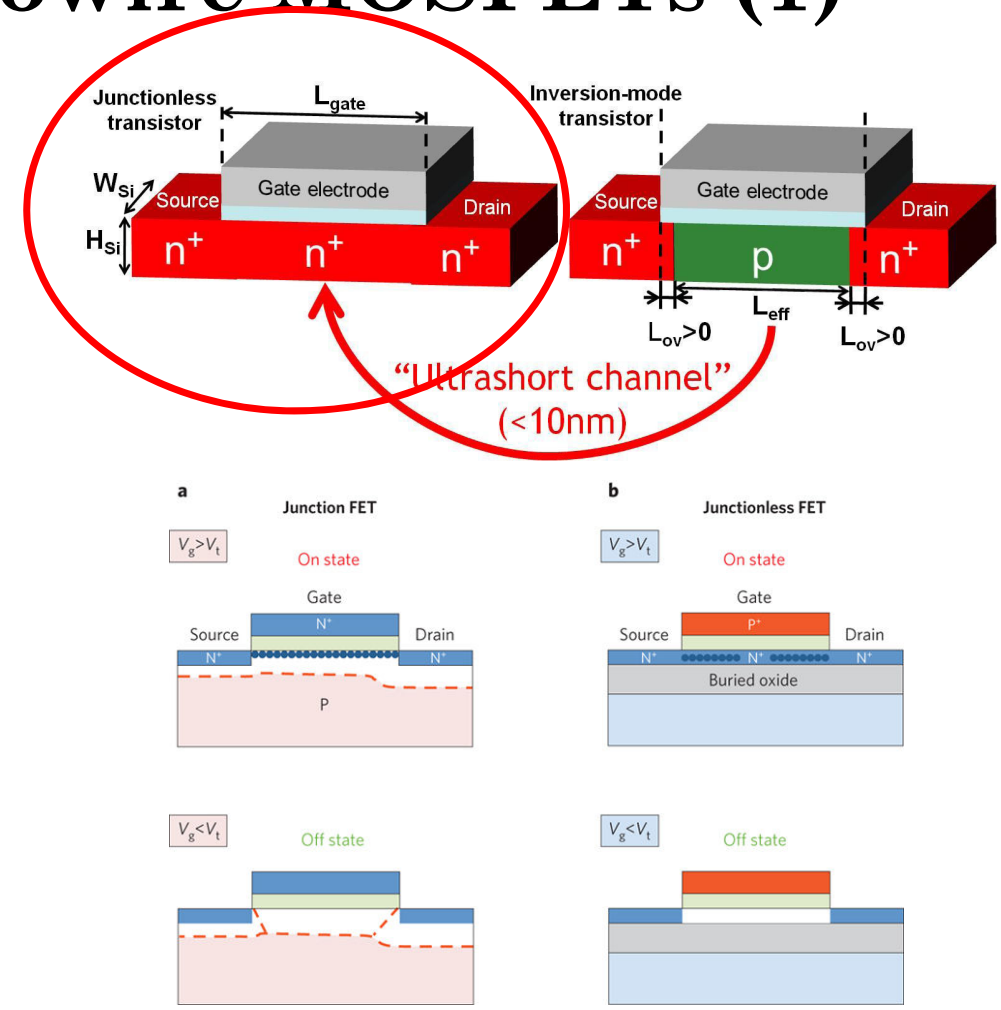
diameters ~5 nm up to ~100 nm

Junctionless nanowire MOSFETs (1)

Operation principle for a junctionless n-type accumulation device:

1. **On-state:** the whole nanowire body behaves as a conducting channel: on current depends on the nanowire's geometry, mobility and doping.
2. **Off-state:** the gate voltage is decreased, the transistor body is gradually depleted, until eventually the transistor turns off.

Merit: much simpler than the junction-based inversion-mode MOSFET and much easier to manufacture.
Challenge: meet performance and variability/manufacturing criteria.



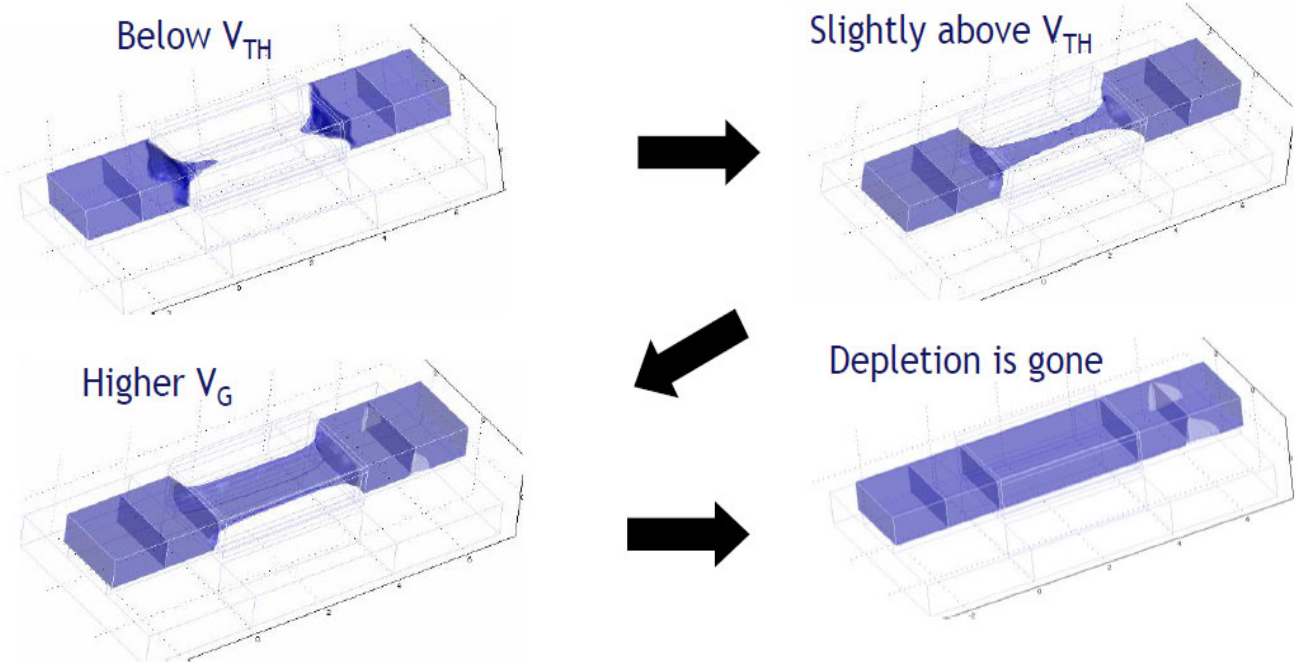
J.P. Colinge et al., Nanowire transistors without junctions, Nature Nanotechnology 5, 225 - 229 (2010)
A.M. Ionescu, Nanowire transistors made easy, Nature Nanotechnology 5, 178 - 179 (2010).

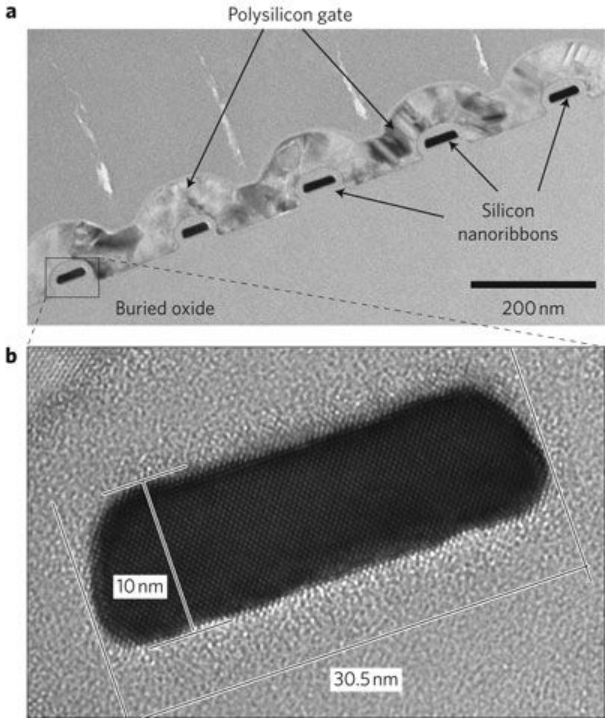
Junctionless nanowire MOSFETs (2)

Electrostatic pinch-off:

The cross section is small enough for the channel region to be depleted

(V_D=50mV, N_d>5e18/cm^3)





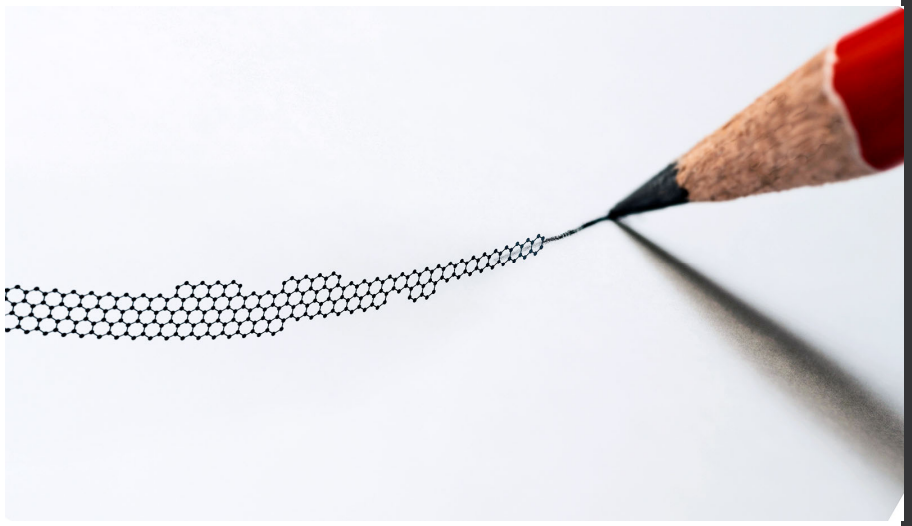
2D Materials Beyond Graphene For Future Electronics

(source of material: Frank Schwierz, Technische Universität Ilmenau, Germany)

Significance of 2D: 1 to few atomic layers

The most well-known 2D material: **Graphene**

- **First 2D material** studied in detail.
- Long history, finally became famous by the works of Novoselov & Geim and Berger & de Heer from 2004.
- **High mobilities (>100 000 cm²/Vs @ 300K)** raised expectations regarding electronic applications (possible successor of Si).



Today:

- The prospects of graphene electronics are considered less optimistic.
- However, significant attention for 2D materials beyond graphene.
- So far, more than 500 layered materials discovered.
- Many of them semiconducting and possibly useful for electronics.

2D Materials –An (Incomplete) Overview

- Graphene, silicene, germanene
- Graphene nanoribbons (GNR)
- Bilayer graphene (BLG)
- Phosphorene, stanene

X-enes

- MQ_2: M = transition metal, Q = chalcogene (S, Se, Te)
- Mo-based TMDs, e.g., MoS_2
- W-based TMDs, e.g., WS_2

2D TMDs

X-anes

- Graphane
- Silicane
- Germanane
- Stanane

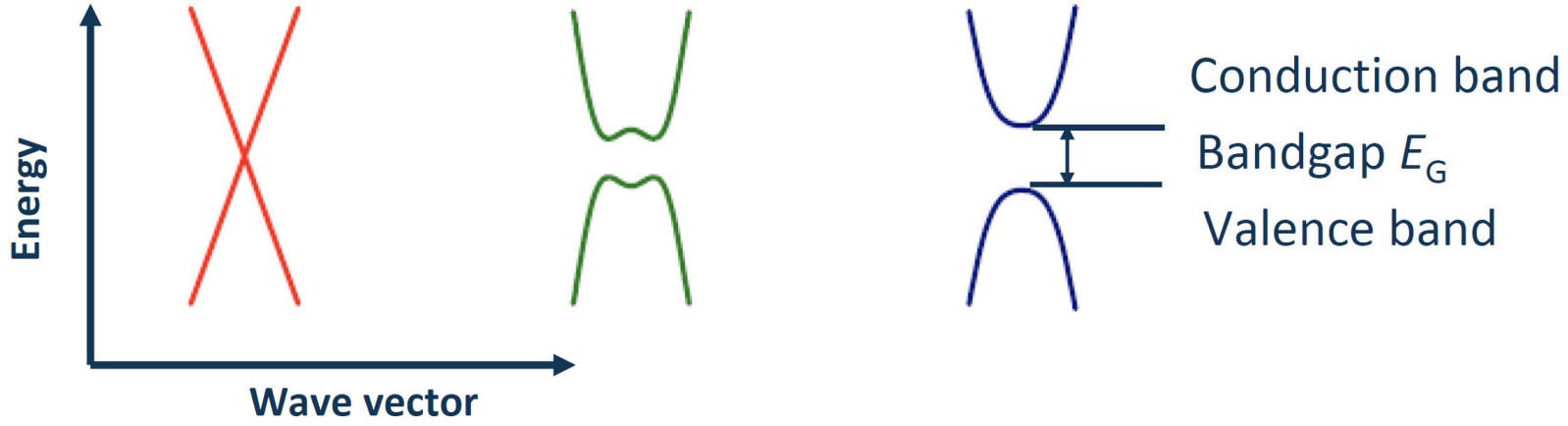
MX-enes

- M_2X: M = early transition metal, X = C or N
- M_2X plus F_2, $(OH)_2$, O_2 e.g. Ti_2CO_2, Sc_2CF_2, …

Many Further 2Ds

Flouro-X-enes, Chloro-X-enes, SMCs, 2D III-Vs, 2D IV-IVs, 2D elementals, etc.

2D Materials – Semiconducting Bandgap



X-enes
- Graphene
- Silicene
- Germanene

No gap, E_G = 0! This is really a pitty, since the missing gap causes serious problems for transistors.

BLG

$E_G \leq 130$ meV
Too narrow for logic transistors.

X-enes
- Phosphorene
- Stanene
- GNRs

X-anes
- Graphane
- Silicane
- Germanane

MX-enes
- Sc_2CF_2
- $TiCO_2$

2D TMDs
- MoS_2, $MoSe_2$, $MoTe_2$
- WS_2, WSe_2, WTe_2

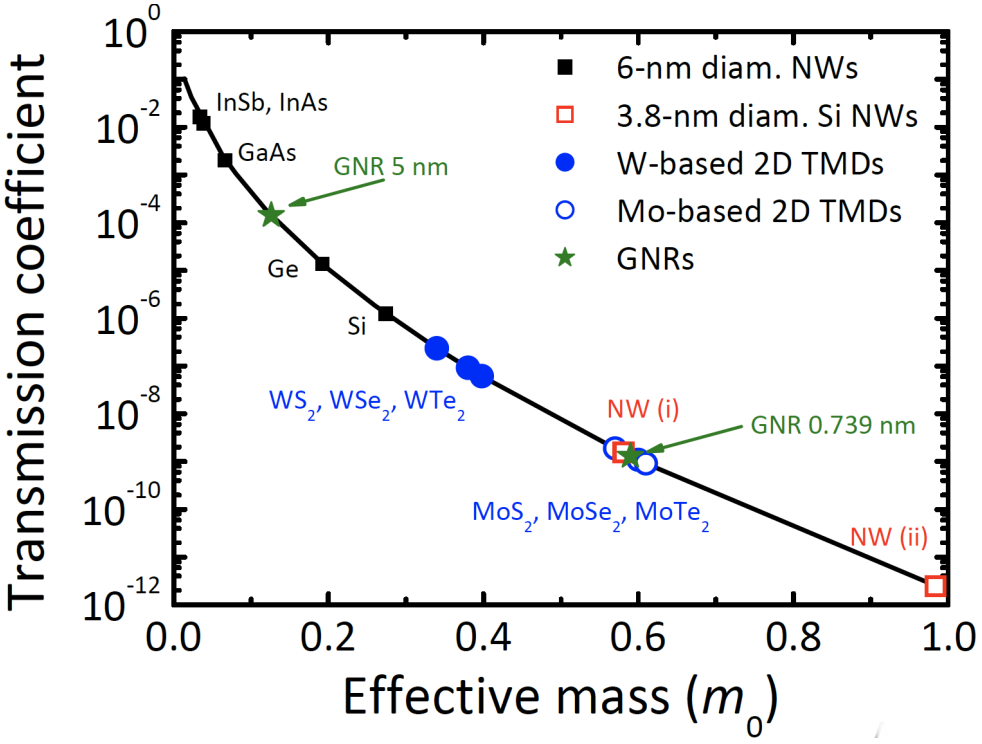
etc., etc.

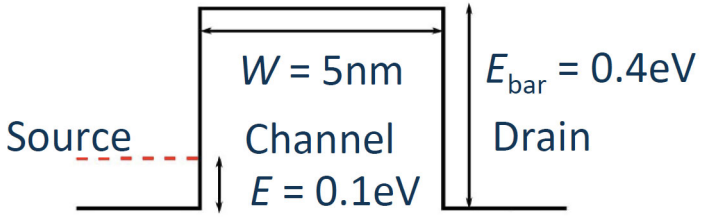
Many of these materials have a gap E_G = 0.5… 2.5 eV, perfect for transistors.

2D Materials for sub-5nm gate length scaling

At 5-nm and below gate lengths:

- Source-drain tunneling will become an issue.
- Tunneling degraded SS and switch-off, high Ioff.
- High-μ, i.e., light-meff narrow-gap channel materials are expected to fail.
- Heavy-meff materials (with lower μ and wider gap) are expected to become favorable.





$$TC = \left[1 + \frac{E_{bar}^2 \sinh\left(|k|W\right)}{4E\left(E_{bar} - E\right)}\right]^{-1}$$

$$k = \sqrt{2 m_{eff}\left(E_{bar} - E\right)} / \hbar$$

$$I_{tun} \approx c \times M \times TC$$

M : Conduction band degeneracy factor
4 for Si and Ge NWs, 1 for III-V NWs.

c: a constant, here 10.4 μA.

DEVICE TECHNOLOGY

MoS_2 transistors with 1-nanometer gate lengths

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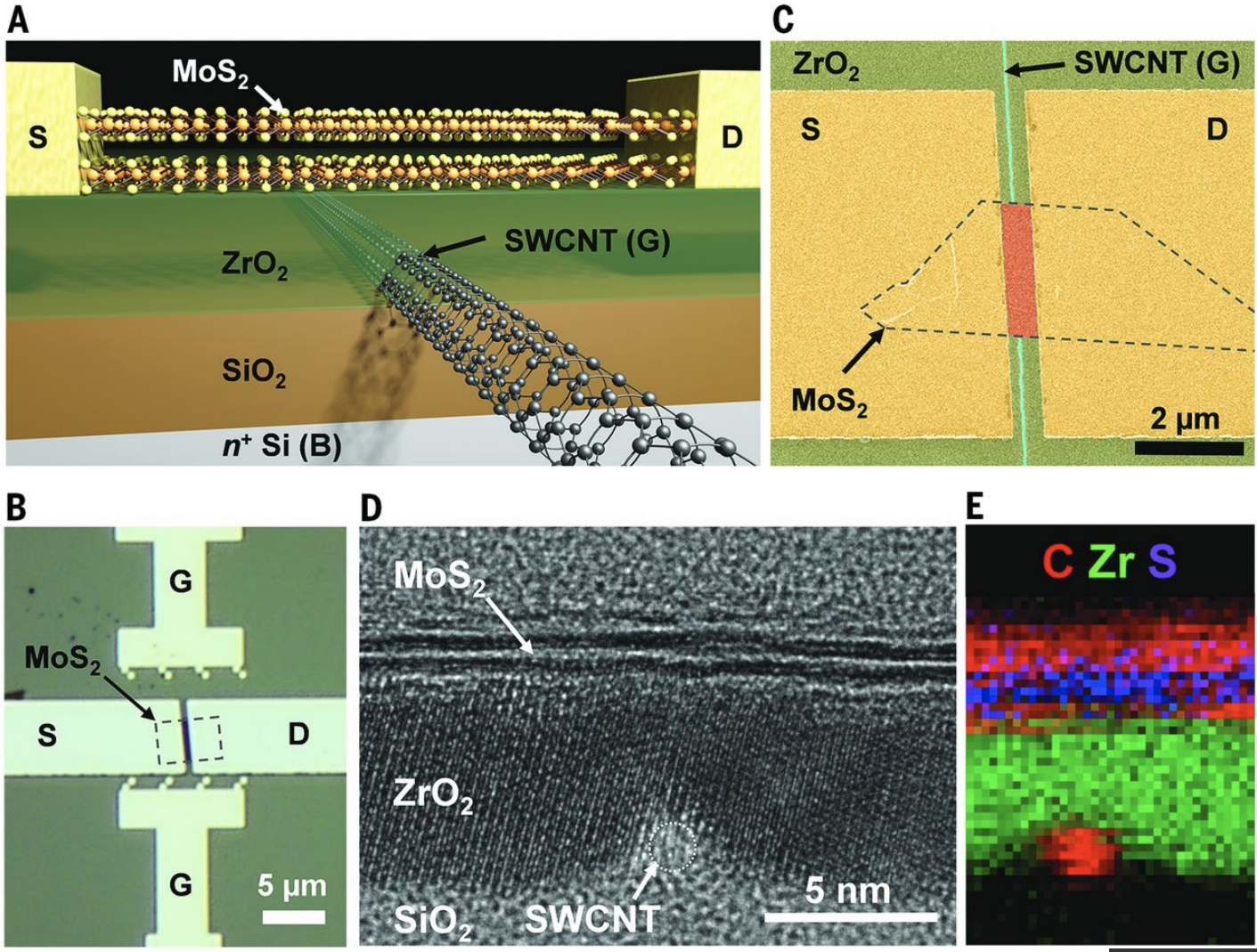
Scaling of silicon (Si) transistors is predicted to fail below 5-nanometer (nm) gate lengths because of severe short channel effects. As an alternative to Si, certain layered semiconductors are attractive for their atomically uniform thickness down to a monolayer, lower dielectric constants, larger band gaps, and heavier carrier effective mass. Here, we demonstrate molybdenum disulfide (MoS_2) transistors with a 1-nm physical gate length using a single-walled carbon nanotube as the gate electrode. These ultrashort devices exhibit excellent switching characteristics with near ideal subthreshold swing of ~65 millivolts per decade and an On/Off current ratio of ~10^6. Simulations show an effective channel length of ~3.9 nm in the Off state and ~1 nm in the On state.



Conclusions

Nanoscale CMOS options:

- 3D devices for best electrostatics: **FinFETs** (current dominant processor technology), deliver best **High Performance** computing solutions
- **Fully-Depleted SOI** as bets solutions for **Low Power comput**ing (future Internet of Things nodes)
- **Below 10 nm;**
  - **Si or III-V Nanowire MOSFET**
  - **2D-material MOSFETs** (other materials than silicon)